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| FORM PTO 1390 (REV 11-2000) U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE | | ATTORNEY'S DOCKET NUMBER |
|---|---|---|
| TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371 | | REGIM-010 |
| | | U S APPLICATION NO (If known, see 37 CFR 1 5) 10/069058 |
| INTERNATIONAL APPLICATION NO. PCT/FR00/02330 | INTERNATIONAL FILING DATES 17 August 2000 | PRIORITY DATE CLAIMED 20 August 1999 |
| TITLE OF INVENTION METHOD FOR TREATING SUBSTRATES FOR MICROELECTRONICS AND SUBSTRATES OBTAINED ACCORDING TO SAID METHOD | | |
| APPLICANT(S) FOR DO/EO/US Thierry Barge, André Auberton-Herve, Hiroji Aga, and Naoto Tate | | |

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information

1. [x] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [ ] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing 35 U.S.C. 371
3. [x] This is an express request to begin national examination procedures (35 U.S.C. 371 (f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. [x] The US has been elected by the expiration of 19 months from the priority date (PCT Article 31).
5. [x] A copy of the International Application as filed (35 U.S.C. 371 (c)(2))
   a. [ ] is attached hereto (required only if not communicated by the International Bureau).
   b. [x] has been communicated by the International Bureau.
   c [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [x] An English language translation of the International Application as filed (35 U.S.C. 371 (c)(2)).
   a. [x] is attached hereto.
   b [ ] has been previously submitted under 35 U S.C. 154(d)(4).
7. [x] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. [ ] are attached hereto (required only if not communicated by the International Bureau).
   b. [ ] have been communicated by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [x] have not been made and will not be made.
8. [ ] An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).
9. [x] An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)). (unexecuted)
10. [x] An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U S.C. 371 (c)(5)).

**Items 11 to 20 below concern document(s) or information included:**

11. [ ] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [ ] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [x] A FIRST preliminary amendment.
14. [ ] A SECOND or SUBSEQUENT preliminary amendment.
15. [ ] A substitute specification.
16. [ ] A change of power of attorney and/or address letter.
17. [ ] A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. [x] A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. [ ] A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. [x] Other items or information: Copy of International Preliminary Examination Report w/annexes (in French & English), Copy of International Search Report (in French & English), Five (5) Sheets of Formal Drawings

JC13 Rec'd PCT/PTO 20 FEB 2002

| U.S. APPLICATION NO (if known, see 37 CFR 1 5) | INTERNATIONAL APPLICATION NO | ATTORNEY'S DOCKET NUMBER |
|---|---|---|
| 10/069058 | PCT/FR00/02330 | REGIM-010 |

21. [X] The following fees are submitted:

**BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) – (5)):**

| | | |
|---|---|---|
| [ ] | Neither international preliminary examination fee (37 CFR 1 482) nor international search fee (37 CFR 1 445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO . | $1040 00 |
| [X] | International preliminary examination fee (37 CFR 1 482) not paid to USPTO but International Search Report prepared by the EPO or JPO | . $890 00 |
| [ ] | International preliminary examination fee (37 CFR 1 482) not paid to USPTO but international search fee (37 CFR 1 445(a)(2)) paid to USPTO . . . | $740 00 |
| [ ] | International preliminary examination fee (37 CFR 1 482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) . . . | $710 00 |
| [ ] | International preliminary examination fee (37 CFR 1 482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) . . . . . | .$100 00 |

**ENTER APPROPRIATE BASIC FEE AMOUNT =** $ 890.00

Surcharge of $ _____ for furnishing the oath or declaration later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492 (e)). $

| CLAIMS | NUMBER FILED | NUMBER EXTRA | RATE | |
|---|---|---|---|---|
| Total claims | *14-20 | | x | $ 0.00 |
| Independent claims | 1-3 = | | x | $ 0.00 |
| MULTIPLE DEPENDENT CLAIM(s) (if applicable) | | | + 280.00 | $ 280.00 |
| **TOTAL OF ABOVE CALCULATIONS =** | | | | $ 1,170.00 |

[ ] Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by ½. $

**SUBTOTAL =** $ 1,170.00

Processing fee of $ _____ for furnishing the English translation later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). + $

**TOTAL NATIONAL FEE =** $ 1,170.00

Fee for recording the enclosed assignment (37 CFR 1.21 (h)). Assignment must be accompanied by appropriate cover sheet (37 CFR 3.28, 3.31) + $
( per property).

**TOTAL FEES ENCLOSED =** $ 1,170.00

*As In IPER

**Amount to be Refunded:** $

**Charged:** $

a. [ ] A check in the amount of $ _____ to cover the above fees is enclosed.

b. [X] Please charge my Deposit Account No. 12-1095 in the amount of $ 1,170.00 to cover the above fees. A duplicate copy of this sheet is enclosed.

c. [X] The Commissioner is hereby authorized to charge any additional fees which may be required or credit any overpayment to my Deposit Account No 12-1095 . A duplicate copy of this sheet is enclosed.

**NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137 (a) or (b)) must be filed and granted to restore the application to pending status.**

SEND ALL CORRESPONDENCE TO

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32,137
REGISTRATION NUMBER

# PROCESS FOR TREATING SUBSTRATES FOR THE MICROELECTRONICS INDUSTRY, AND SUBSTRATES OBTAINED BY THIS PROCESS

The invention relates to the field of processes for treating substrates intended for the manufacture of microelectronic and/or optoelectronic components.

The invention also relates to the substrates obtained by this process.

More specifically, the invention relates to the field of processes for treating substrates that are entirely semiconductors (for example silicon) or entirely insulators, or alternatively substrates that consist of a stack of semiconducting or insulating layers. These may be substrates onto which is deposited a layer (for example an epitaxial layer) or substrates comprising nonhomogeneous structures, such as substrates comprising components or parts of components at more or less advanced levels of their production.

There exists, to a certain depth from the surface of at least one face of these substrates, a layer of material which, at least partially, makes up the constitution of the components prepared on this face. This layer will be referred to hereinbelow by the expression "working layer".

The quality of this working layer conditions that of the components. Efforts are continually being made to improve the quality of this working layer. Thus, attempts are made both to reduce the surface roughness of this working layer and to reduce the concentration of defects in the thickness of this layer.

It is known that chemical-mechanical polishing methods can be used to reduce the surface roughness of the working layer.

It is also known that chemical-mechanical polishing techniques can be used to reduce the concentration of certain defects in the working layer, when a concentration gradient of these defects exists,

increasing in the direction of the surface of this layer. In this case, the chemical-mechanical polishing abrades the working layer down as far as the zones, deeper than the initial surface of the working layer, which have an acceptable concentration of these defects.

However, it is also known that chemical-mechanical polishing causes a degradation of certain properties of the working layer and a reduction in the capacity to produce substrates (FR 2 762 136 and FR 2 761 526).

It has thus been proposed to replace chemical-mechanical polishing, in particular when the working layer consists of silicon, with an annealing operation in a hydrogen-containing atmosphere (FR 2 762 136 and FR 2 761 526). An annealing, under a hydrogen-containing atmosphere, of substrates comprising a working layer consisting of silicon has an effect of reducing the surface roughness, in particular by reconstructing the silicon surface, as well as a role of healing certain crystal defects.

One aim of the invention is to further improve the quality of the working layer.

This aim is achieved, according to the invention, by means of a process for treating substrates for the microelectronics or optoelectronics industry, comprising a working layer on at least one of their faces, this process comprising a step of chemical-mechanical polishing on the free surface of the working layer, characterized in that it also comprises a step of annealing under a reductive atmosphere, before the polishing step.

It is well known that chemical-mechanical polishing causes certain defects in the material lying underneath the polished surface and is liable to give rise to nonuniform thicknesses of the substrates, and in particular of the working layer.

However, surprisingly, the Applicant has found that by preceding the chemical-mechanical polishing step with an annealing operation under a reductive atmosphere, not only can the quality of the working layer be improved more effectively than by simple polishing or simple annealing, but also most of the harmful effects of a simple chemical-mechanical polishing are avoided. This is because the annealing operation under a reductive atmosphere has already begun to make the surface of the working layer smooth. The polishing time required to obtain a satisfactory roughness is thus reduced. As a result, the process according to the invention makes it possible to increase the production capacities. In addition, the reduction in the polishing time limits the negative effects of the polishing, such as those mentioned above, or the loss of uniformity of thickness which generally arises when the polishing lasts a long time.

Thus, the quality, in terms of roughness of the working layer, after carrying out the process according to the invention, is particularly advantageous.

The roughness measurements are generally carried out by means of an atomic force microscope. With this type of apparatus, the roughness is measured on areas scanned by the tip of the atomic force microscope, going from 1×1 $\mu m^2$ to 10×10 $\mu m^2$ and, more rarely, 50×50 $\mu m^2$ or even 100×100 $\mu m^2$. The roughness can be characterized, in particular, according to two modes. According to one of these modes, the roughness is said to be high-frequency roughness and corresponds to scanned areas of the order of 1×1 $\mu m^2$. According to another of these modes, the roughness is said to be low-frequency roughness and corresponds to scanned areas of the order of 10×10 $\mu m^2$, or more.

Chemical-mechanical polishing and annealing under a reductive atmosphere are distinguished by their effects on different ranges of frequencies. Thus, annealing under a reductive atmosphere promotes

smoothing-out of the high-frequency roughness, but is less efficient for reducing the undulations, which are, rather, low-frequency. Chemical-mechanical polishing, on the other hand, makes it possible also to improve the low-frequency roughness.

By means of the process according to the invention, low high-frequency roughness can be obtained, by means of the annealing operation under a reductive atmosphere, and small undulations, i.e. a type of low-frequency roughness, can be obtained by means of the polishing operation. Now, low high-frequency roughness is fundamental for obtaining good screen oxides, and low undulation (low-frequency roughness) is advantageous when it is desired to bond another substrate to the free surface of the working layer.

In addition to its effect on roughness, the process according to the invention makes it possible to reduce the concentration of certain defects in the working layer. Specifically, the annealing operation under a reductive atmosphere makes it possible to begin reconstructing the surface of the working layer and to heal certain defects in the thickness of the working layer. However, this healing can only be partial. Nevertheless, if the chemical-mechanical polishing operation is continued for long enough, it allows removal of the material comprising a large proportion of the defects in the region of the free surface of the working layer and in the thickness of this working layer. The process according to the invention is thus particularly advantageous when there is an increasing concentration gradient in the direction of the free surface of the working layer, and a high concentration of defects in the region of this surface. The combined effect of healing the defects, by the annealing operation under a reductive atmosphere, and of removing material, by the polishing operation, allows a

particularly effective removal of the defects in the region of the free surface of the working layer.

By means of the process according to the invention, a substrate is thus obtained with a working layer whose quality is sufficient and compatible with the use of this working layer in microelectronic or optoelectronic applications.

The reductive atmosphere advantageously comprises hydrogen. This reductive atmosphere also preferentially comprises argon.

Thus, the reductive atmosphere can be composed of 100% hydrogen. However, advantageously, the reductive atmosphere is composed of a mixture of hydrogen and argon. This mixture is preferentially in an $H_2$/Ar ratio of 20/80 or of 25/75. With ratios of this type, the hydrogen is in a sufficient concentration to be significant, but, by virtue of the argon, the mixture is a better heat conductor. The enhancement of the heat-conducting properties of the mixture reduces the thermal constraints on the substrate. This results in a smaller generation of defects of sliding-band type. This type of mixture is also less corrosive, which results in a less selective attack of certain defects.

Advantageously also, the process according to the invention additionally comprises a sacrificial oxidation step. This sacrificial oxidation step comprises a step of oxidizing the working layer over at least a portion of its thickness and a step of deoxidizing this oxidized portion. The oxidation and deoxidation steps can be carried out after the polishing step and/or before it.

A sacrificial oxidation step is advantageously carried out to improve the quality of a working layer, whether the material constituting this working layer is a material which is readily oxidized or not readily oxidized. In the text hereinbelow, and in particular in the claims, a sacrificial oxidation step will be

considered as achievable whether or not the material of the working layer is readily oxidized.

Each of the polishing and sacrificial oxidation steps participates in removing the portion of the working layer comprising an excessive concentration of defects. However, a sacrificial oxidation step, subsequent to the polishing step, more specifically participates in deleting the surface defects generated by the polishing step.

A sacrificial oxidation step also limits other deleterious effects of the polishing operation. Specifically, if a relatively thick layer of defects is present at the start, a long polishing time is required to remove it. However, a long polishing time generally results in a lack of thickness uniformity. This drawback is all the more critical the thicker the material to be removed and thus the longer the polishing step lasts. Furthermore, long polishing operations slow down the execution of the process and induce a limitation on the production capacity. By introducing a sacrificial oxidation step in the process according to the invention, these drawbacks are avoided by limiting the polishing operation essentially to that which is required to reduce the roughness, the sacrificial oxidation step contributing appreciably towards removing the part of the working layer comprising a high concentration of defects. Furthermore, by reducing the polishing required, the defects thereby generated may be developed on a smaller scale.

Advantageously also, the process according to the invention comprises at least one heat treatment step, the step of oxidizing the working layer being carried out before the end of each of these heat treatment steps, in order to protect the rest of the working layer. Under these conditions, the heat treatment can also at least partially heal the defects generated during the oxidation step.

Advantageously also, the process according to the invention additionally comprises a step of annealing under a reductive atmosphere after the polishing step.

Advantageously also, the process according to the invention comprises a step of implanting atoms under one face of a wafer, in an implantation zone, a step of placing the face of the wafer, which has undergone the implantation, in intimate contact with a support substrate, and a step of cleaving the wafer in the implantation zone, in order to transfer some of the wafer onto the support substrate and form a thin film or a thin layer thereon, this thin film or this thin layer constituting the working layer which is then subjected to the steps of annealing in hydrogen and of polishing.

Advantageously also, the process according to the invention is carried out on a substrate comprising a working layer consisting of a semiconductor material. This semiconductor material is, for example, silicon.

Advantageously also, and in particular if the working layer consists of silicon, the step of annealing under a reductive atmosphere is carried out according to a known procedure described, for example, in document FR 2 761 526. According to this procedure, the substrate is annealed at a temperature of between about 1050°C and 1350°C, for a few tens of seconds to a few tens of minutes, under a hydrogen-containing atmosphere.

According to another advantageous variant of the process according to the invention, the step of annealing under a reductive atmosphere is carried out according to another known procedure described, for example, in document EP 917 188. According to this other procedure, the substrate is annealed, under a hydrogen-containing atmosphere, at a temperature of between about 1100°C and 1300°C, in less than three minutes, preferably in less than 60 seconds and even

more preferably in less than thirty seconds. This other procedure corresponds to a rapid annealing operation, also known as RTA annealing (RTA being the acronym for the expression Rapid Thermal Annealing).

The annealing operation can be carried out at constant temperature, at variable temperature, with temperature stages, or a combination of stages and variable ranges.

According to yet another advantageous variant of the process according to the invention, the step of annealing under a reductive atmosphere is carried out according to another known procedure described, for example, in document FR 2 761 526. According to this other procedure, the substrate is annealed in apparatus which produces a hydrogen plasma. The advantage of this type of annealing lies in the fact that the annealing temperature is low. This temperature is typically within a range from room temperature to about 600°C.

With a working layer consisting of silicon, whether the annealing step under a hydrogen-containing atmosphere is carried out in a long annealing operation, an annealing operation in a hydrogen plasma or carried out in an annealing operation of RTA type, it has several effects. These effects are:

- a disintegration of the native oxide at the surface of the working layer;

- an etching of the silicon ($SiH_2$ and $SiH_4$ being volatile), leading to a reduction in the average thickness of the working layer;

- a healing of certain defects by dissolving the oxygen precipitates and other oxide walls capable of playing a stabilizing role on certain crystal defects; but also

- a smoothing and a reduction of the roughness of the surface of the working layer, with the appearance of terraces at the atomic scale.

In particular, the disintegration of the silicon oxides with hydrogen greatly facilitates the reorganization of the silicon atoms.

At the surface in particular, the silicon atoms, activated by the annealing operation under a hydrogen-containing atmosphere, migrate at the surface until they find themselves in an energy configuration corresponding to an increased stability. Thus, the silicon atoms present in excrescences have a tendency to migrate into cavities. In this way, the step of annealing under a hydrogen-containing atmosphere has a tendency to reduce the surface roughness.

As regards the healing of certain defects, the effect of dissolving the oxygen precipitates and other oxide walls is particularly advantageous in the case of defects known as "COPs" (the acronym for the expression Crystal Originated Particles). These "COP" defects are collections of lacunae which are of the order of a few hundred to a few thousand angstroms in size and whose oriented walls, which are oriented in crystal planes, are stabilized with oxides in a thickness of the order of not more than a few tens of angstroms. These "COP" defects appear in particular in CZ silicon.

According to another aspect, the invention is a substrate for the microelectronics or optoelectronics industry, comprising a working layer on at least one of its faces, this substrate having been obtained after a step of chemical-mechanical polishing on the free surface of the working layer, characterized in that it has also undergone a step of annealing under a reductive atmosphere, before the polishing step.

Other aspects, aims and advantages of the invention will become apparent on reading the detailed description which follows. The invention will also be better understood with the aid of the attached drawings, in which:

- Figure 1 diagrammatically shows, in longitudinal cross section, an example of a chamber for

carrying out each step of annealing under a hydrogen-containing atmosphere, of the process according to the invention;

- Figure 2 diagrammatically shows, in cross section along a plane perpendicular to its main surfaces, a substrate in the course of its treatment by the process in accordance with the present invention;

- Figure 3 diagrammatically shows, in cross section along a plane perpendicular to its main surfaces, a substrate in the course of its treatment by a variant of the process in accordance with the present invention;

- Figure 4 diagrammatically shows, in cross section along a plane perpendicular to its main surfaces, a substrate in the course of its treatment by another variant of the process in accordance with the present invention;

- Figure 5 diagrammatically shows, in cross section along a plane perpendicular to its main surfaces, a substrate in the course of its treatment by yet another variant of the process in accordance with the present invention; and

- Figure 6 diagrammatically shows, in cross section along a plane perpendicular to its main surfaces, a substrate in the course of its treatment by yet another variant of the process in accordance with the present invention.

Five embodiments of the process in accordance with the present invention are described below, as detailed examples.

These five embodiments are illustrated below as examples, but without any limiting nature, in the context of the manufacture of silicon on insulator substrates. The silicon on insulator substrates are also referred to as SOI substrates.

In this context, the process according to the invention finds a particularly advantageous application

in the manufacture of SOI substrates by processes of a particular type, known as SMART-CUT® processes.

One particular way of carrying out a SMART-CUT® process is described in patent FR 2 681 472.

In the context of the manufacture of SOI substrates, a SMART-CUT® process produces substrates comprising a working layer 52 consisting of silicon on one face thereof, this silicon layer resting on a layer of insulator, also known as the layer of buried oxide 56.

According to one of its variants, the SMART-CUT® process comprises:

- a step of implanting atoms, under one face of a semiconductor wafer, in an implantation zone;
- a step of placing the wafer subjected to the implantation in intimate contact with a support substrate; and
- a step of cleaving the wafer in the implantation zone, in order to transfer the portion of the wafer located between the surface subjected to the implantation and the implantation zone, onto the said support substrate and to form a thin film, or a layer, of silicon thereon.

The expression "implanting atoms" means any bombardment of atomic or ionic species which is capable of introducing these species into a material, with a concentration maximum for these species in this material, this maximum being located at a given depth relative to the bombarded surface. The atomic or ionic species are introduced into the material with an energy also distributed around a maximum. The implantation of the atomic species into the material can be carried out by means of an ion-beam implanter, a plasma-immersion implanter, etc.

The term "cleavage" means any fracture of the implanted material at the concentration maximum, in this material, of the implanted species or in the region of this maximum. This fracture does not

necessarily occur along a crystallographic plane of the implanted material.

Several approaches may be envisaged to prepare an SOI substrate according to the SMART-CUT® process.

According to a first approach, a silicon wafer is covered on its implantation face with a layer of insulating oxide (for example by oxidation of the silicon), and a support substrate, for example one also made of silicon, is used for the transfer.

According to a second approach, a layer which is entirely made of semiconductor (of silicon) is transferred either onto a support substrate covered with a layer of insulator or onto a support substrate which is entirely made of insulator (for example quartz).

According to a third approach, a layer covered with an insulating layer is transferred either onto a support substrate also covered with insulator, or onto a support substrate which is entirely made of insulator.

After cleavage and transfer, an SOI substrate 50 with a layer transferred onto one face of the support substrate is obtained in all cases, the free surface of this layer corresponding to a cleavage surface. After cleavage, the substrate 50 is freed of dust, cleaned and rinsed according to the usual techniques used in microelectronics.

In this case, it is advantageous to use the process according to the invention to reduce the roughness of the said free surface and the density of defects in the transferred layer.

According to the process in accordance with the present invention, the SOI substrate 50 undergoes a step of annealing under a reductive atmosphere 100 and a polishing step 200.

For all the embodiments described below, the step of annealing under a reductive atmosphere is

carried out according to the RTA procedure described above.

An example of a chamber for carrying out a step of annealing under a reductive atmosphere 100, according to the RTA procedure, is illustrated in Figure 1.

This chamber 1 comprises an enclosure 2, a reactor 4, a substrate-holder wafer 6, two arrays of halogen lamps 8, 10 and two pairs of side lamps.

The enclosure 2 in particular comprises a bottom wall 12, a top wall 14 and two side walls 16, 18, respectively located at the longitudinal ends of the enclosure 2. One of the side walls 16, 18 comprises a door 20.

The reactor 4 consists of a quartz tube extending longitudinally between the two side walls 16, 18. Each of these side walls 16, 18, respectively, is fitted with a gas inlet 21 and a gas outlet 22. The gas outlet 22 is on the side of the side wall 18 comprising the door 20.

Each array of halogen lamps 8, 10 is respectively located above and below the reactor 4, between this reactor and the bottom 12 and top 14 walls. Each array of halogen lamps 8, 10 comprises 17 lamps 26 arranged perpendicular to the longitudinal axis of the reactor 4. The two pairs of side lamps (not represented in Figure 1) are located parallel to the longitudinal axis of the reactor 4, each on one side of this reactor, globally at the longitudinal ends of the lamps 26 of the arrays of halogen lamps 8, 10.

The substrate-holder wafer 6 slides in the reactor 4. It supports the substrates 50 which are intended to undergo the step of annealing under a hydrogen-containing atmosphere 100 and allows them to be placed in or removed from the chamber 1.

A chamber 1 of this type is sold by STEAG® under the name "SHS AST 2800".

The five embodiments of the process according to the invention, described below, are applied to the treatment of SOI substrates 50 comprising a working layer 52 itself having a free surface 54. This free surface 54 is a cleavage surface obtained, as described above, by carrying out a SMART-CUT® process. Under the working layer 52, the substrate 50 comprises a layer of buried oxide 56. Under the layer of buried oxide 56, the substrate 50 comprises a support substrate 58.

The parameters given for the five embodiments of the process according to the invention, which will be described below, correspond to "fine product" applications. These "fine products" are SOI substrates whose silicon on insulator layer, i.e. the working layer 52, is about 2000 Å thick, whereas the layer of buried insulator 56 is about 4000 Å thick. To prepare SOI substrates having a thicker working layer 52 and/or a thicker layer of buried oxide, an implantation operation at higher energy will be carried out, in order for the layer of atomic species implanted to be located deeper down than the bombarded surface. In this case, it will also have to be taken into account that the deeper the atomic species are implanted, the more material it will be necessary to remove after cleavage, in order to regain an acceptable concentration of defects in the working layer 52. The reason for this is that the deeper the atomic species are implanted, the more the width of the defective zone increases.

According to the first embodiment, represented in Figure 2, a substrate 50 is subjected, after the cleavage step of the SMART-CUT® process described above and a cleaning operation, to a step of annealing under a reductive atmosphere 100, and then to a step of chemical-mechanical polishing 200.

Before these two steps, the concentration of defects 59 in the working layer 52, in the region of the free surface 54, and the roughness of this surface are unsatisfactory.

The step of annealing under a reductive atmosphere 100 is carried out according to the RTA-type procedure described above.

The step of annealing under a reductive atmosphere consists in:

- placing the substrate 50 in a chamber 1 such as the one described above, this chamber being cold when the substrate 50 is introduced;

- introducing, at a pressure equal to or in the region of atmospheric pressure, a mixture of hydrogen and argon, in proportions by volume of 25% hydrogen to 75% argon;

- increasing, by lighting the halogen lamps 26, the temperature in the chamber 1, at a rate of about 50°C per second, up to a treatment temperature;

- keeping the substrate 50 in the chamber 1, for 20 seconds, at the treatment temperature, this treatment temperature advantageously being chosen between 1200°C and 1230°C and preferably being equal to 1230°C; and

- switching off the halogen lamps 26 and cooling, by circulation of air, the substrate 50, at a rate of several tens of degrees centigrade per second and varying according to the temperature range.

Under these conditions, with rapid heating and cooling ramps, and a short steady stage, this annealing operation under a reductive atmosphere 100 reduces the roughness virtually without removing material. The thickness of material removed is less than 20 Å. The reduction in the roughness is essentially achieved by surface reconstruction and smoothing rather than by etching. In addition, the crystal defects 59 in the silicon of the working layer 52, generated during the implantation and cleavage operations, are at least partly healed by this annealing operation under a reductive atmosphere 100. The concentration of these defects 59, in the working layer 52, is thus reduced. Consequently, the thickness of working layer 52, over

which the concentration of defects 59 is too great to be acceptable, is reduced. Furthermore, the fact that this annealing operation is performed under a reductive atmosphere 100, according to the RTA procedure, prevents propagation of the attack of certain defects down as far as the layer of buried oxide 56.

The annealing step under a reductive atmosphere 100 described above offers many other advantages. It is readily compatible with a high production capacity for the substrates 50, is easy to use, can be carried out with already-existing equipment, etc.

The roughness is generally expressed either in terms of the difference between the minimum height and the maximum height measured during scanning of the surface whose roughness is measured, or by means of a root mean square (rms) value. The difference between the minimum and maximum heights will be denoted hereinbelow by "P-V" (from the term "Peak-Valley").

After the step of annealing under a reductive atmosphere 100, the roughness measured during scanning of a 1×1 $\mu m^2$ area is reduced from 50 to 1-1.5 Å rms (i.e. from a value of greater than 500 Å to about 20 Å, in P-V values), and the roughness measured during scanning of a 10×10 $\mu m^2$ area is reduced from 50 to 5-15 Å rms (i.e. from a value of greater than 500 Å to 40-50 Å in P-V value).

The polishing step 200 is carried out by a conventional chemical-mechanical polishing operation known to those skilled in the art. Starting with a surface which has already been made quite smooth by the step of annealing under a reductive atmosphere 100, a polishing step 200 on a thickness of 200 to 400 Å only is sufficient to bring the roughness, and more particularly the low-frequency roughness, to a satisfactory value. Typically, the roughness after polishing is from about 0.8 to 1.5 Å rms, if this measurement is carried out during scanning of a 1×1 $\mu m^2$

area, or from about 1 to 2 Å rms if this measurement is carried out during scanning of a 10×10 $\mu m^2$ area.

This polishing step 200 also makes it possible to remove from the working layer 52 the material lying close to the free surface 54 and comprising defects 59.

The second embodiment of the process according to the invention is represented in Figure 3. By way of example, as previously, it is carried out on a substrate 50 of SOI type obtained after the cleavage step of the SMART-CUT® process described above and a cleaning operation.

According to this second embodiment, the substrate 50 is subjected to an annealing step under a reductive atmosphere 100A, then to a chemical-mechanical polishing step 200A and finally to a sacrificial oxidation step 300A combined with a heat treatment 320A.

The steps of annealing under a reductive atmosphere 100A and of chemical-mechanical polishing 200A in this embodiment are identical to those described for the first embodiment.

The sacrificial oxidation step 300A is intended to remove the defects 59 remaining after the polishing step 200A. These defects 59 may arise from the implantation, from the cleavage, or may have been generated during the polishing step 200A, etc.

The sacrificial oxidation step 300A is made up of an oxidation step 310A and a deoxidation step 330A. The heat treatment 320A comes between the oxidation step 310A and the deoxidation step 330A.

The oxidation step 310A is preferably carried out at a temperature of between 700°C and 1100°C. The oxidation step 310A can be carried out via a dry route or a wet route. Via a dry route, the oxidation step 310A is carried out, for example, by heating the substrate 50 under oxygen gas. Via a wet route, the oxidation step 310A is carried out, for example, by heating the substrate 50 under an atmosphere charged

with water vapor. Via a wet or dry route, according to conventional processes known to those skilled in the art, the oxidative atmosphere can also be charged with hydrochloric acid.

The oxidation step 310A results in the formation of an oxide 60.

The heat treatment step 320A is carried out by any thermal operation intended to improve the qualities of the material constituting the working layer 52. This heat treatment 320A can be carried out at constant temperature or at variable temperature. In the latter case, the heat treatment 320A is carried out, for example, with a gradual increase of the temperature between two values, or with a cyclic oscillation between two values, etc.

The heat treatment step 320A is preferably carried out at least partly at a temperature above 1000°C and more particularly at about 1100-1200°C.

The heat treatment step 320A is preferably carried out under a nonoxidative atmosphere. The atmosphere for the heat treatment 320A can comprise argon, nitrogen, hydrogen, etc., or alternatively a mixture of these gases. The heat treatment 320A can also be carried out under vacuum.

Preferably also, the oxidation step 310A is carried out before the heat treatment step 320A. In this way, the oxide 60 protects the rest of the working layer during the heat treatment 320A and prevents the phenomenon of pitting. The phenomenon of pitting is well known to those skilled in the art. It occurs at the surface of certain semiconductors when they are annealed under a nonoxidative atmosphere, such as nitrogen, argon, under vacuum, etc. It occurs in the case of silicon in particular when the latter is laid bare, i.e. when it has no oxide coat at all.

According to one advantageous variant, the oxidation step 310A begins with the start of the

temperature increase of the heat treatment 320A and finishes before the end of this heat treatment.

The heat treatment 320A makes it possible to heal, at least partly, the defects generated during the preceding steps of the process for manufacturing and treating the substrate 50. More particularly, the heat treatment 320A can be carried out for a time and at a temperature such that crystal defects are thereby healed, such as stacking faults, "HF" defects, etc., generated in the working layer 52 during the oxidation step 310A. The term "HF" defect refers to a defect whose presence is revealed by a decorative halo in the buried oxide 56, after treating the substrate 50 in a hydrofluoric acid bath.

The heat treatment 320A also has the advantage of reinforcing the bonding interface, for example between the layer transferred during the transfer by the SMART-CUT® process and the support substrate 58.

The deoxidation step 330A is preferably carried out in solution. This solution is, for example, a 10% or 20% hydrofluoric acid solution. A few minutes suffice to remove from one thousand to several thousand angstroms of oxide 60, by immersing the substrate 50 in such a solution.

During this second embodiment of the process according to the invention, the following will be removed:

- at least 15 Å of silicon from the working layer 52, during the step of annealing under a reductive atmosphere 100,
- 300 Å of silicon from the working layer 52, during the polishing step 200, and
- 650 Å of silicon from the working layer 52, during the sacrificial oxidation step 300.

The total thickness of working layer 52 removed during the process according to the invention, in this second embodiment, is equal to about 950 Å. In general, the second embodiment of the process according to the

invention will advantageously make it possible to remove 800 to 1100 Å.

Table 1 collates the roughnesses measured after the various steps of the second embodiment of the process according to the invention.

| | 1×1 $\mu m^2$ area scanned | | 10×10 $\mu m^2$ area scanned | |
|---|---|---|---|---|
| | P-V roughness (Å) | rms roughness (Å) | P-V roughness (Å) | rms roughness (Å) |
| After cleavage | 500/1000* | 50/100* | 500/1000* | 50/100* |
| After the step of annealing under a reductive atmosphere 100 | 10/30 | 1-1.5 | 40-50 | 5-15 |
| After the polishing step 200 | 10 | 0.8-1.5 | 10 | 1-2 |
| After the sacrificial oxidation step 300 | 10 | 0.8-1.5 | 10 | 1-2 |

*: After cleavage, the surface is so rough that the roughness cannot be measured significantly with an atomic force microscope.

**Table 1: Roughnesses measured after the various steps of the second embodiment of the process according to the invention.**

The third embodiment of the process according to the invention is represented in Figure 4. By way of example, and as for the preceding embodiments, it is carried out on a substrate 50 of SOI type obtained after the cleavage step of the SMART-CUT® process described above and a cleaning operation.

After the cleavage step and a cleaning operation, the substrate 50 is subjected to:

- a first sacrificial oxidation step 301B combined with a heat treatment 321B,
- a step of annealing under a reductive atmosphere 100B,

- a chemical-mechanical polishing step 200B, and

- a second sacrificial oxidation step 302B combined with a heat treatment 322B.

The steps of annealing under a reductive atmosphere 100B and of chemical-mechanical polishing 200B in this embodiment are identical to those described for the first embodiment described above.

The first and second sacrificial oxidation steps 301B, 302B are made up, like the sacrificial oxidation step 300A described above, of an oxidation step 311B, 312B and a deoxidation step 331B, 332B. The first and second sacrificial oxidation steps 301B, 302B, and the heat treatment steps 321B, 322B, are similar to those already described for the second embodiment, described above, of the process in accordance with the present invention.

During this third embodiment of the process according to the invention, the following will be removed:

- 650 Å of silicon from the working layer 52, during the first sacrificial oxidation step 301B,

- less than 15 Å of silicon from the working layer 52, during the step of annealing under a reductive atmosphere 100B,

- 300 Å of silicon from the working layer 52, during the polishing step 200B, and

- 650 Å of silicon from the working layer 52, during the second sacrificial oxidation step 302B.

The total thickness of working layer removed during the process according to the invention, in this third embodiment, is equal to about 1600 Å.

Table 2 collates the roughnesses measured after the various steps of the second embodiment of the process according to the invention.

| | 1×1 $\mu m^2$ area scanned | | 10×10 $\mu m^2$ area scanned | |
|---|---|---|---|---|
| | P-V | rms | P-V | rms |

| | roughness (Å) | roughness (Å) | roughness (Å) | roughness (Å) |
|---|---|---|---|---|
| After cleavage | 500-1000* | 50-100* | 500-1000* | 50-100* |
| After the first sacrificial oxidation step 301B | 250-500 | 25-50 | 300-600 | 30-60 |
| After the step of annealing under a reductive atmosphere 100B | 20 | 1-1.5 | 40-50 | 5-10 |
| After the polishing step 200B | 10 | 0.8-1.5 | 10 | 1-2 |
| After the second sacrificial oxidation step 302B | 10 | 0.8-1.5 | 10 | 1-2 |

*: After cleavage, the surface is so rough that the roughness cannot be measured significantly with an atomic force microscope.

**Table 2: Roughnesses measured after the various steps of the third embodiment of the process according to the invention.**

The fourth embodiment is represented in Figure 5. By way of example, and as for the preceding embodiments, it is carried out on a substrate 50 of SOI type obtained after the cleavage step of the SMART-CUT® process described above.

After the cleavage step and a cleaning operation, the substrate 50 is subjected to:

- a step of annealing under a reductive atmosphere 100C,
- a first sacrificial oxidation step 301C combined with a heat treatment 321C,
- a chemical-mechanical polishing step 200C, and
- a second sacrificial oxidation step 302C combined with a heat treatment 322C.

The steps of annealing under a reductive atmosphere 100C and of chemical-mechanical polishing 200C in this embodiment are identical to those described for the first embodiment described above.

The first and second sacrificial oxidation steps 301C, 302C are made up, as for the sacrificial oxidation step 300A described above, of an oxidation step 311C, 312C and a deoxidation step 331C, 332C.

The first and second sacrificial oxidation steps 301C, 302C, and the heat treatment steps 321C, 322C, are similar to those already described for the second embodiment, described above, of the process in accordance with the present invention.

During this fourth embodiment of the process according to the invention, the following will be removed:

- less than 15 Å of silicon from the working layer 52, during the step of annealing under a reductive atmosphere 100C,
- 650 Å of silicon from the working layer 52, during the first sacrificial oxidation step 301C,
- 300 Å of silicon from the working layer 52, during the polishing step 200C, and
- 650 Å of silicon from the working layer 52, during the second sacrificial oxidation step 302C.

The total thickness of working layer 52 removed during the process according to the invention, in this fourth embodiment, is equal to about 1600 Å.

Table 3 collates the roughnesses measured after the various steps of the fourth embodiment of the process according to the invention.

| | 1×1 $\mu m^2$ area scanned | | 10×10 $\mu m^2$ area scanned | |
|---|---|---|---|---|
| | P-V roughness (Å) | rms roughness (Å) | P-V roughness (Å) | rms roughness (Å) |
| After cleavage | 500-1000* | 50-100* | 500-1000* | 50-100* |
| After the step of annealing under a | 10-30 | 1-1.5 | 40-50 | 5-15 |

| | | | | |
|---|---|---|---|---|
| reductive atmosphere 100C | | | | |
| After the first sacrificial oxidation step 301C | 10-30 | 1-1.5 | 40-50 | 5-15 |
| After the polishing step 200C | 10 | 0.8-1.5 | 10 | 1-2 |
| After the second sacrificial oxidation step 302C | 10 | 0.8-1.5 | 10 | 1-2 |

*: After cleavage, the surface is so rough that the roughness cannot be measured significantly with an atomic force microscope.

**Table 3: Roughnesses measured after the various steps of the fourth embodiment of the process according to the invention.**

The fifth embodiment is represented in Figure 6. By way of example, and as for the preceding embodiments, it is carried out on a substrate 50 of SOI type obtained after the cleavage step of the SMART-CUT® process described above.

After the cleavage step and a cleaning operation, the substrate 50 is subjected to:

- a first step of annealing under a reductive atmosphere 101D,
- a chemical-mechanical polishing step 200D, and
- a second step of annealing under a reductive atmosphere 102D.

The steps of annealing under a reductive atmosphere 101D, 102D and of chemical-mechanical polishing 200D in this embodiment are identical to those described for the first embodiment.

During this fifth embodiment of the process according to the invention, the following will be removed:

- less than 15 Å of silicon from the working layer 52, during the first step of annealing under a reductive atmosphere 101D,
- 400 Å of silicon from the working layer 52, during the polishing step 200D, and
- less than 15 Å of silicon from the working layer 52, during the second step of annealing under a reductive atmosphere 102D.

The total thickness of working layer 52 removed during the process according to the invention, in this fifth embodiment, is equal to about 400 Å.

According to one variant of this fifth embodiment of the process according to the invention, a heat treatment such as those already described or alternatively a sacrificial oxidation combined with a heat treatment, such as those also described above, can be inserted into the fifth embodiment described above.

Table 4 collates the roughnesses measured after the various steps of the fifth embodiment of the process according to the invention.

| | 1×1 $\mu m^2$ area scanned | | 10×10 $\mu m^2$ area scanned | |
|---|---|---|---|---|
| | P-V roughness (Å) | rms roughness (Å) | P-V roughness (Å) | rms roughness (Å) |
| After cleavage | 500-1000* | 50-100* | 500-1000* | 50-100* |
| After the first step of annealing under a reductive atmosphere 101D | 10-30 | 1-1.5 | 40-50 | 5-15 |
| After the polishing step 200D | 10 | 0.8-1.5 | 10 | 1-2 |
| After the second step of annealing under a reductive atmosphere 102D | 10 | 0.8-1.5 | 10 | 1-2 |

*: After cleavage, the surface is so rough that the roughness cannot be measured significantly with the atomic force microscope.

**Table 4: Roughnesses measured after the various steps of the fifth embodiment of the process according to the invention.**

This fifth embodiment of the process according to the invention is particularly advantageous when the surface roughness after cleavage is reduced. This is the case in particular when the implantation is carried out with several energies (FR 2 774 510) and/or with several atomic species or alternatively when the cleavage is accompanied by mechanical constraints (FR 2 748 851).

CLAIMS

1. A process for treating substrates (50) for the microelectronics or optoelectronics industry, comprising on at least one of their faces a working layer (52) in which components are intended to be formed, this process comprising a step of chemical-mechanical polishing on the free surface (54) of the working layer (52), which also comprises a step of annealing under a reductive atmosphere (100, 100A, 100B, 100C, 101D, 102D), before the polishing step (200, 200A, 200B, 200C, 200D).

2. The process as claimed in claim 1, wherein the step of annealing under a reductive atmosphere is carried out in less than three minutes, preferably in less than sixty seconds and even more preferably in less than thirty seconds.

3. The process as claimed in either of the preceding claims, wherein the step of annealing under a reductive atmosphere is carried out at a temperature of between 1100°C and 1300°C, and preferably between 1200°C and 1230°C.

4. The process as claimed in one of the preceding claims, which also comprises, after the polishing step (200, 200A, 200B, 200C, 200D), a step (310A, 312B, 312C) of oxidizing the working layer (52) over at least a portion of its thickness.

5. The process as claimed in one of the preceding claims, which also comprises, before the polishing step (200, 200A, 200B, 200C, 200D), a step (311B, 311C) of oxidizing the working layer (52) over at least a portion of its thickness.

6. The process as claimed in either of claims 4 and 5, which also comprises at least one oxide removal step (330A, 331B, 332B, 331C, 332C).

7. The process as claimed in one of claims 4 to 6, which also comprises at least one heat treatment step (320A, 321B, 322B, 321C, 322C), the step of oxidizing

the working layer (52) being carried out before the end of each heat treatment step (320A, 321B, 322B, 321C, 322C), in order to protect the rest of the working layer (52).

8. The process as claimed in one of the preceding claims, which also comprises a step of annealing under a reductive atmosphere (102D) after the polishing step (200, 200A, 200B, 200C, 200D).

9. The process as claimed in one of the preceding claims, which comprises a step of implanting atoms under one face of a wafer, in an implantation zone, a step of placing the face of the wafer, which has undergone the implantation, in intimate contact with a support substrate, and a step of cleaving the wafer in the implantation zone, in order to transfer some of the wafer onto the support substrate and form a thin film or a thin layer thereon, this thin film or this thin layer constituting the working layer (52) which is then subjected to the steps of annealing under a reductive atmosphere (100, 100A, 100B, 100C, 101D, 102D) and of polishing (200, 200A, 200B, 200C, 200D).

10. The process as claimed in one of the preceding claims, wherein the working layer (52) consists of a semiconductor.

11. The process as claimed in claim 10, wherein the semiconductor is silicon.

12. The process as claimed in one of the preceding claims, wherein the reductive atmosphere comprises hydrogen.

13. The process as claimed in one of the preceding claims, wherein the reductive atmosphere comprises argon.

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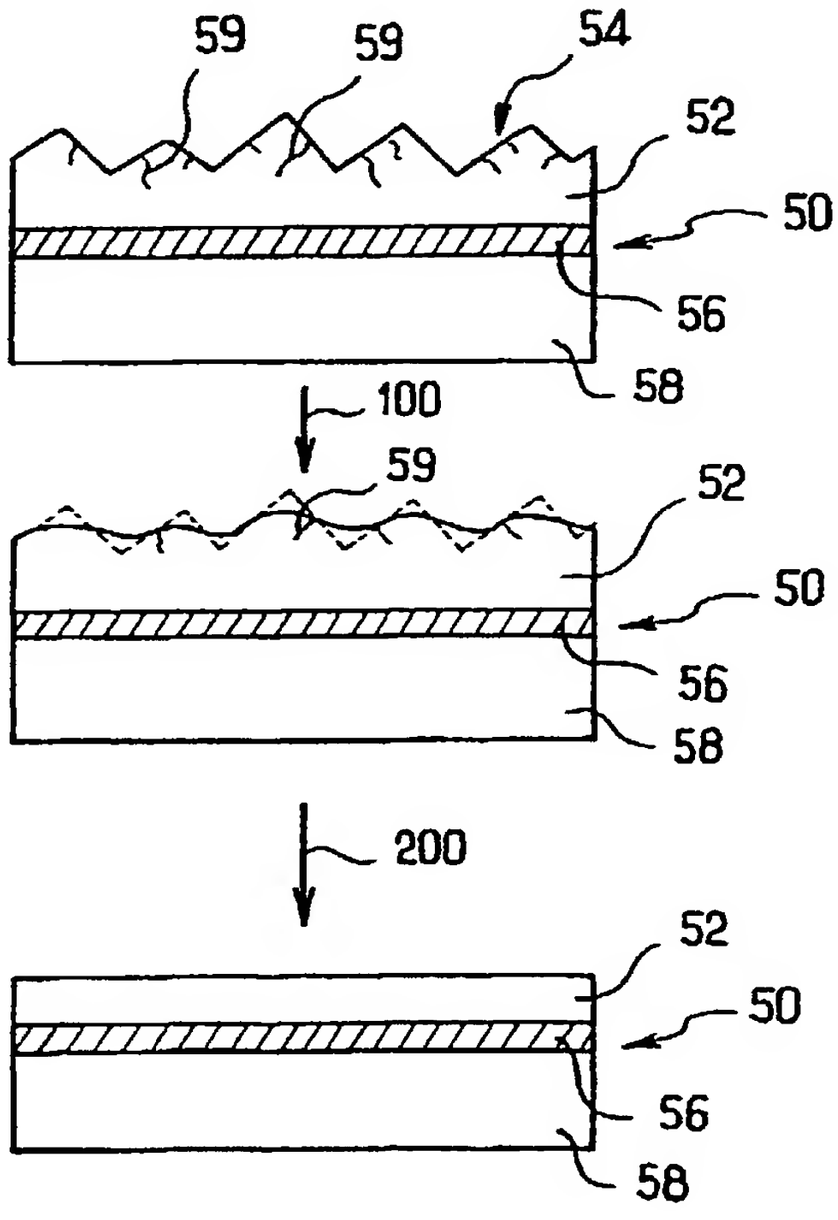
*[Suite sur la page suivante]*

(54) Title: METHOD FOR TREATING SUBSTRATES FOR MICROELECTRONICS AND SUBSTRATES OBTAINED ACCORDING TO SAID METHOD

(54) Titre: PROCEDE DE TRAITEMENT DE SUBSTRATS POUR LA MICRO-ELECTRONIQUE ET SUBSTRATS OBTENUS PAR CE PROCEDE




(57) Abstract: The invention relates to a method for treating substrates (50) for microelectronics or optoelectronics, whereby said substrates comprise a useful layer (52) on at least one of the surfaces thereof. The inventive method includes a mechanical/chemical polishing step occurring on a bare surface (54) of the useful layer and is characterized in that it also comprises a post-curing step in a reductive atmosphere (100) before said polishing step occurs.

(57) Abrégé: L'invention concerne un procédé de traitement de substrats (50) pour la micro-électronique ou l'opto-électronique, comportant une couche utile (52) sur au moins une de leurs faces, ce procédé comprenant une étape de polissage mécano-chimique sur la surface libre (54) de la couche utile (52), caractérisé en ce qu'il comprend en outre, une étape de recuit sous atmosphère réductrice (100), avant l'étape de polissage (200). Elle concerne également des substrats obtenus par ce procédé.

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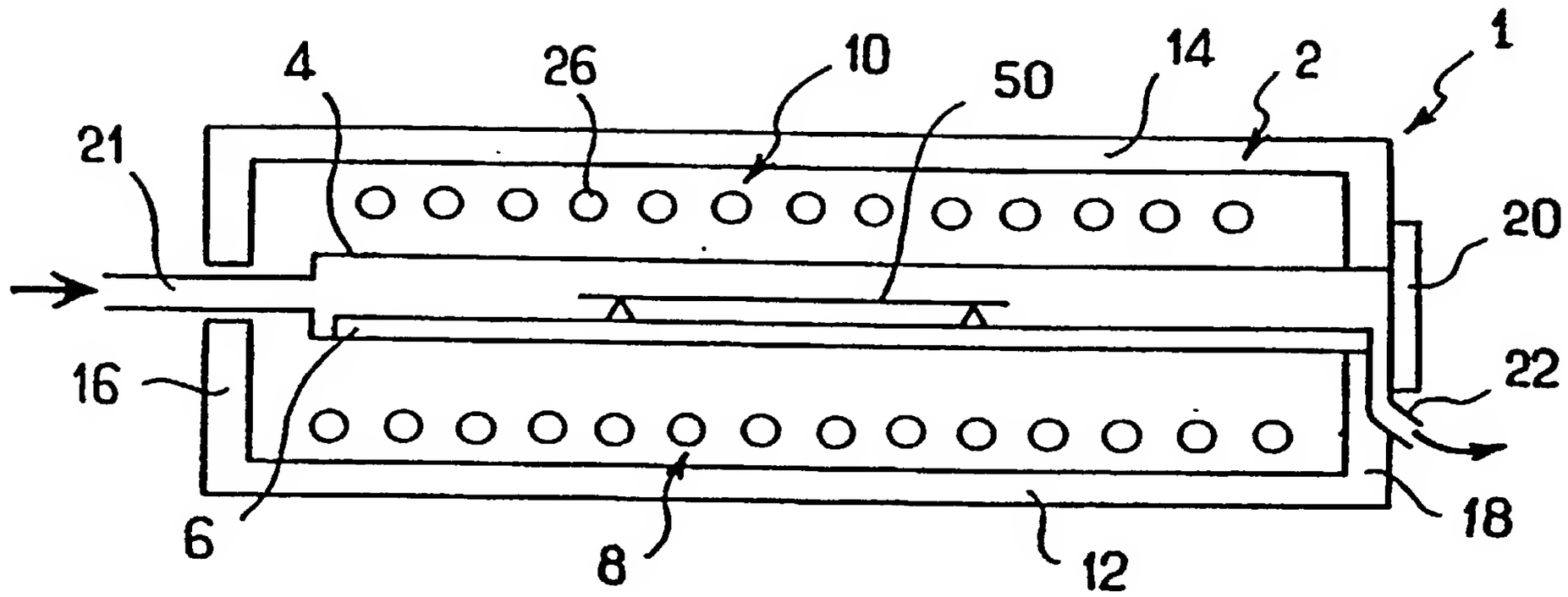
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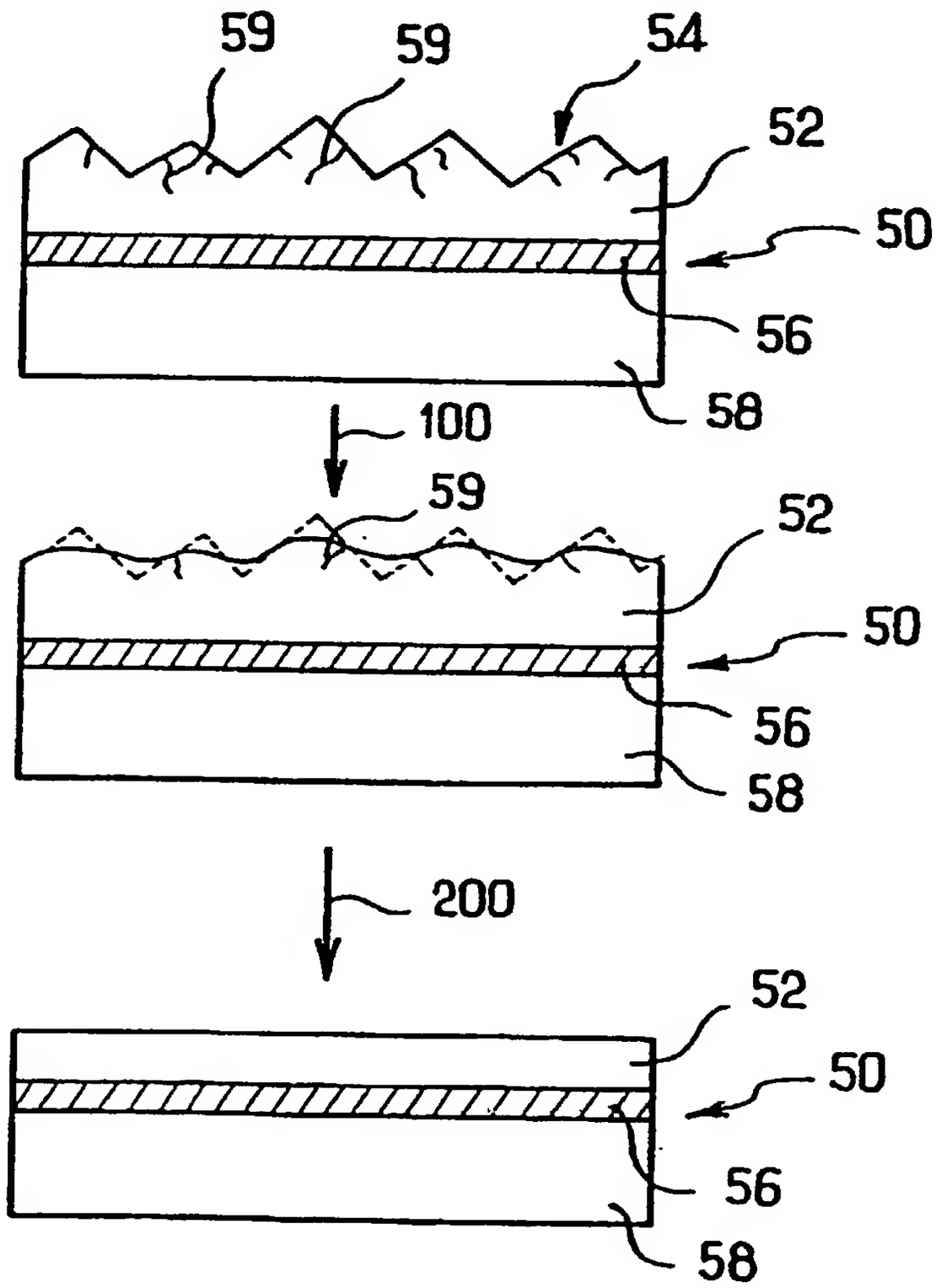
FIG_1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100
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200
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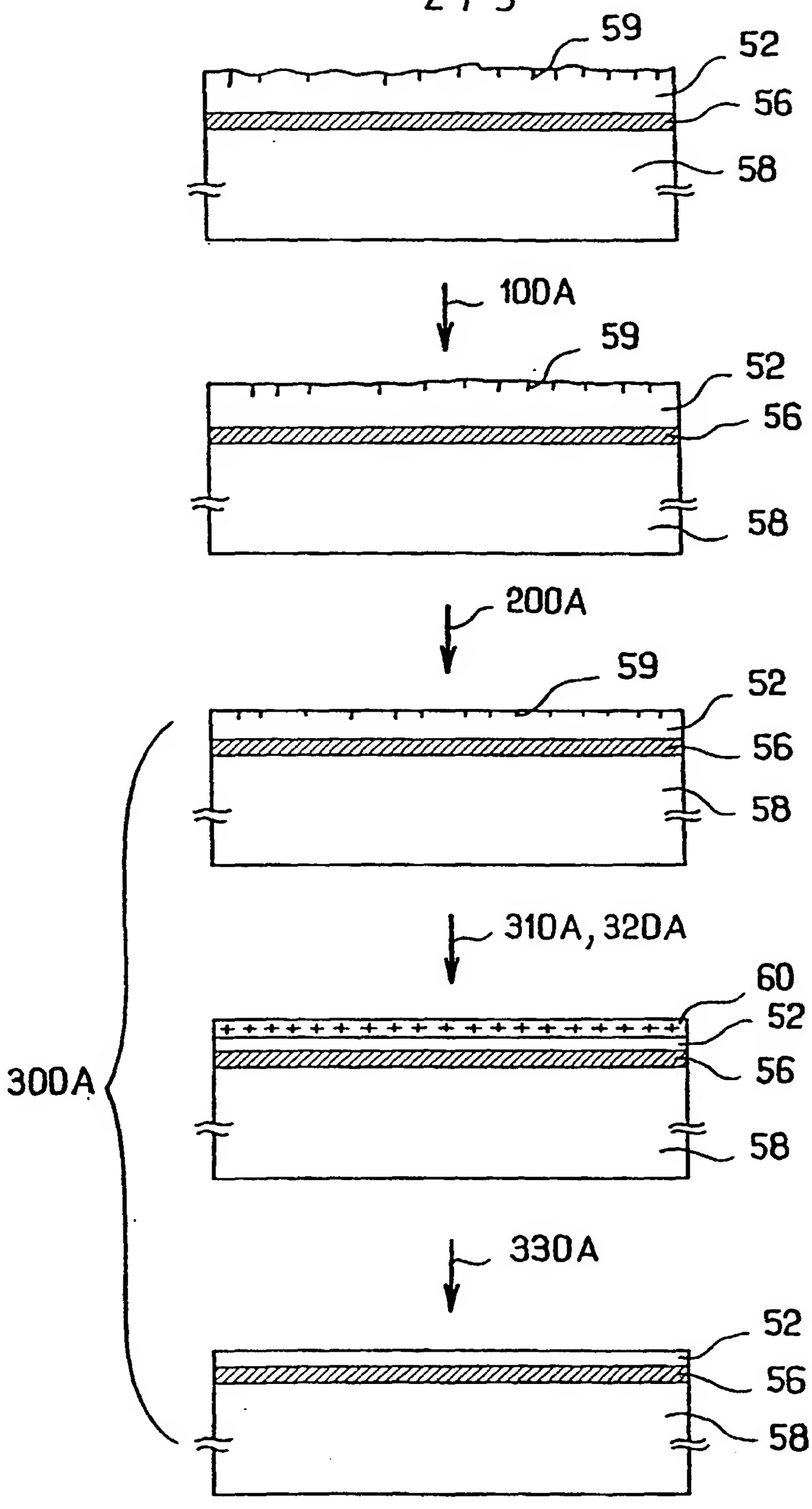
FIG_2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100A
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200A
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310A, 320A
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330A
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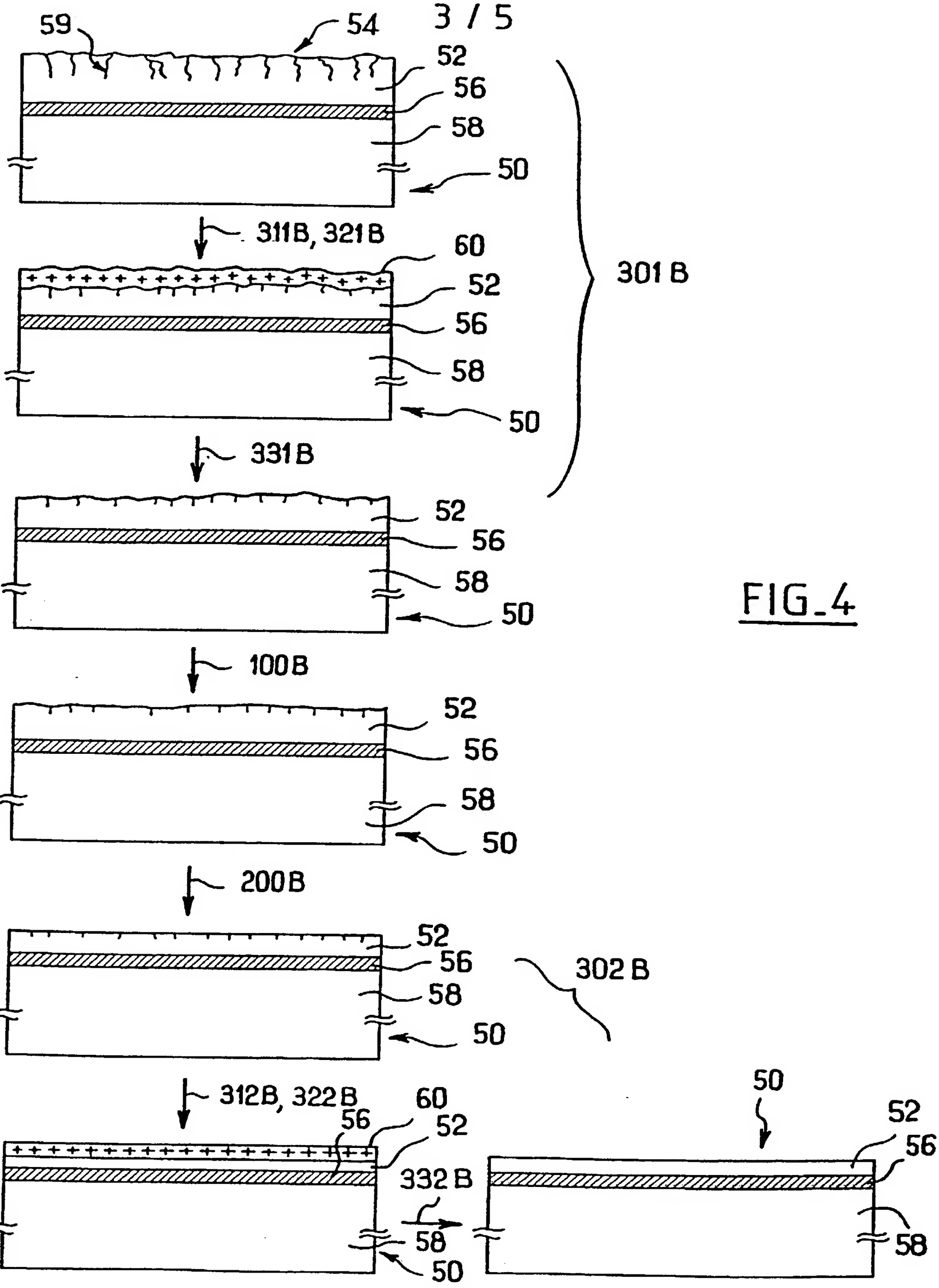
FIG_3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311B, 321B
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301B
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56
58
50
200B
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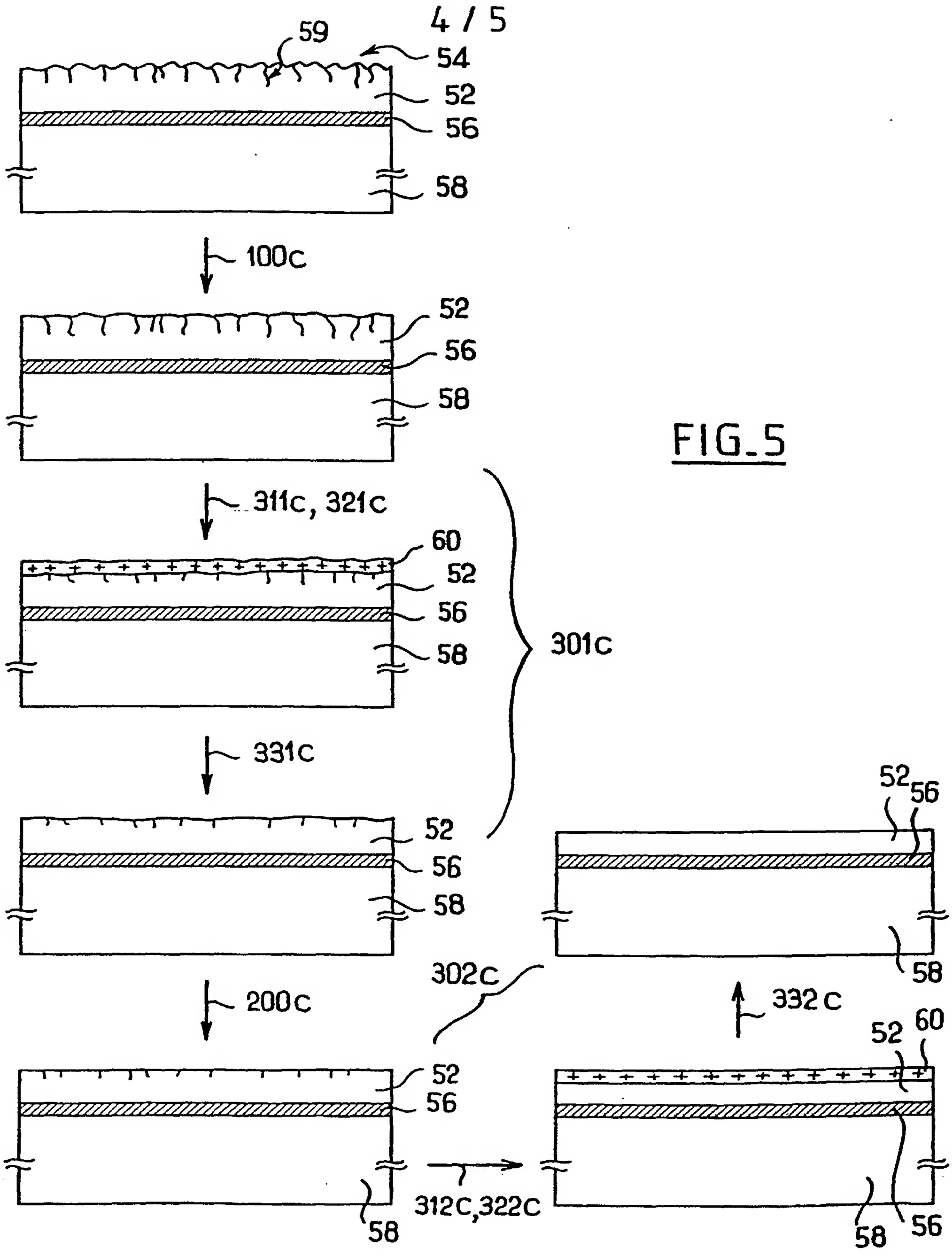
FIG_4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311c, 321c
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301c
331c
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200c
332 c
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312c,322c

FIG_5

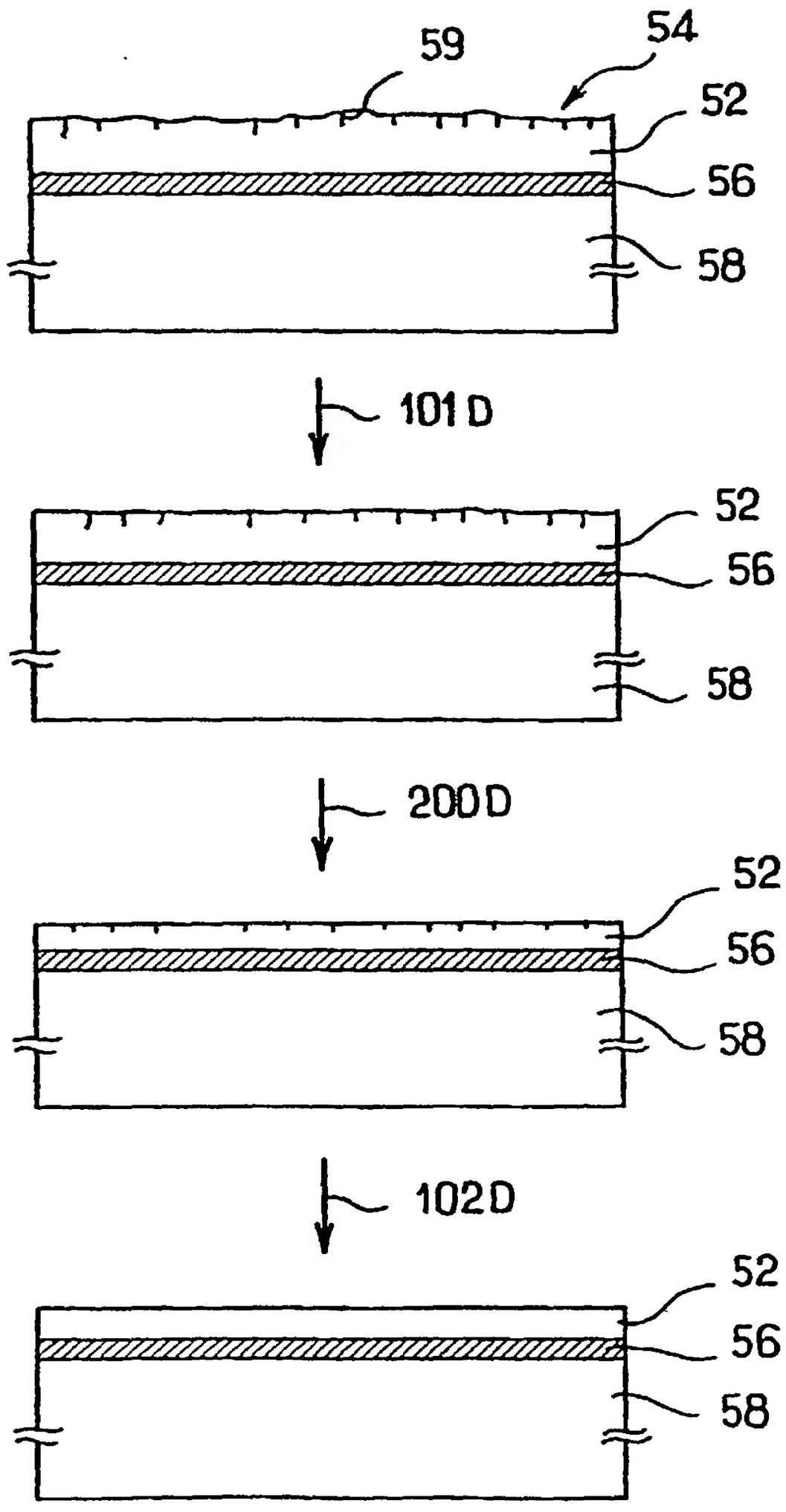


FIG_6

#4

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# DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

[ ] Declaration Submitted with Initial Filing OR [X] Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)

| | |
|---|---|
| Attorney Docket Number | REGIM 3.3-010 |
| First Named Inventor | Thierry Barge |
| *COMPLETE IF KNOWN* | |
| Application Number | UNKNOWN |
| Filing Date | February 20, 2002 |
| Group Art Unit | N/A |
| Examiner Name | Not Yet Assigned |

**As a below named inventor, I hereby declare that:**

My residence, mailing address, and citizenship are as stated below next to my name.

I believe I am the original and first inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD FOR TREATING SUBSTRATES FOR MICROELECTRONICS AND SUBSTRATES OBTAINED ACCORDING TO SAID METHOD

*(Title of the Invention)*

the specification of which

[ ] is attached hereto

OR

[X] was filed on (MM/DD/YYYY) 08/17/2000 as United States Application Number or PCT International Application No. PCT/FR00/02330 and was amended on (MM/DD/YYYY) 10/26/2001 (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365 (a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or of any PCT international application having a filing date before that of the application on which priority is claimed.

| Prior Foreign Application Number(s) | Country | Foreign Filing Date (MM/DD/YYYY) | Priority Not Claimed | Certified Copy Attached? YES | NO |
|---|---|---|---|---|---|
| 99/10667 | FR | 08/20/1999 | [ ] | [ ] | [X] |
| | | | [ ] | [ ] | [ ] |
| | | | [ ] | [ ] | [ ] |
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[ ] Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

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# DECLARATION — Utility or Design Patent Application

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: Customer Number 000530

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Name

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Country | Telephone | Fax

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

**NAME OF SOLE OR FIRST INVENTOR:** [ ] A petition has been filed for this unsigned inventor

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Inventor's Signature | Date August 12, 2002

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Inventor's Signature | Date August 12, 2002

Residence: City St. Egreve | State | Country France | Citizenship France FRX

Mailing Address: 94, avenue de Karben

City St. Egreve | State | ZIP 38120 | Country France

[X] Additional inventors are being named on the 1 supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto.

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# DECLARATION

**ADDITIONAL INVENTOR(S)**
**Supplemental Sheet**
Page 1 of 1

**Name of Additional Joint Inventor, if any:** ☐ A petition has been filed for this unsigned inventor

| | | | |
|---|---|---|---|
| Given Name (first and middle [if any]) 3-00 Hiroji | | Family Name or Surname Aga | |
| Inventor's Signature Hiroji Aga | | | Date August 12, 2002 |
| Residence: City Annaka Gunma | State | Country Japan | Citizenship Japan JPX |
| Mailing Address: 3-12-37-B-115 Isobe | | | |
| City Annaka Gunma | State | ZIP 379-0127 | Country Japan |

**Name of Additional Joint Inventor, if any:** ☐ A petition has been filed for this unsigned inventor

| | | | |
|---|---|---|---|
| Given Name (first and middle [if any]) 4-00 Naoto | | Family Name or Surname Tate | |
| Inventor's Signature Naoto Tate | | | Date August 12, 2002 |
| Residence: City Annaka Gunma | State | Country Japan | Citizenship Japan JPX |
| Mailing Address: 3315-10 Itahana | | | |
| City Annaka Gunma | State | ZIP 379-0111 | Country Japan |

**Name of Additional Joint Inventor, if any:** ☐ A petition has been filed for this unsigned inventor

| | | | |
|---|---|---|---|
| Given Name (first and middle [if any]) | | Family Name or Surname | |
| Inventor's Signature | | | Date |
| Residence: City | State | Country | Citizenship |
| Mailing Address: | | | |
| City | State | ZIP | Country |

**Name of Additional Joint Inventor, if any:** ☐ A petition has been filed for this unsigned inventor

| | | | |
|---|---|---|---|
| Given Name (first and middle [if any]) | | Family Name or Surname | |
| Inventor's Signature | | | Date |
| Residence: City | State | Country | Citizenship |
| Mailing Address: | | | |
| City | State | ZIP | Country |